

PTO-1449 (Modified) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT BY APPLICANT	ATTY. DOCKET NO. RA043D2DC	SERIAL NUMBER 09/545,648
	APPLICANT(S) FARMWALD ET AL.	
	FILING DATE April 10, 2000	GROUP ART UNIT 2181



U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
<i>MA</i>	5,034,964	Jul. 23, 1991	Khan et al	—	—	

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO
<i>MA</i>	SHO 58-192154	Nov. 9, 1983	Japan	—	—	NO
<i>MA</i>	SHO 63-34795	Feb. 15, 1988	Japan	—	—	NO
<i>MA</i>	SHO 61-107453	May 26, 1986	Japan	—	—	NO
<i>MA</i>	SHO 63-91766	April 22, 1988	Japan	—	—	YES
<i>MA</i>	SHO 62-16289	Jan. 24, 1987	Japan	—	—	NO
<i>MA</i>	SHO 61-160556	Oct. 4, 1986	Japan	—	—	NO

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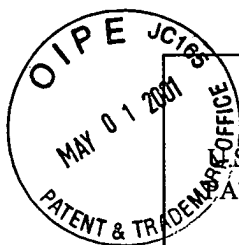
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EXAMINER <i>Glenn Anne</i>	DATE CONSIDERED <i>4/3/2001</i>
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ON	4,755,937	July 5, 1989	Glier			
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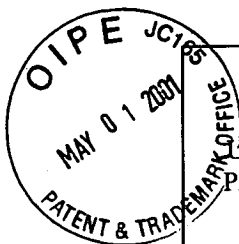
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ON	Pelgrom et al., "A 32-kbit Variable-Length Shift Register for Digital Audio Application", IEEE Journal of Solid-State Circuits, vol. sc-22, no. 3, June 1987, pp 415-422
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ON	Gustavson et al., "The Scalable Interface Project (Superbus)" (DRAFT), SCI-22 Aug 88-doc1 pp 1-16, August 22, 1988
ON	Knut Alnes, "SCI: A Proposal for SCI Operation", SCI-10Nov88-doc23, Norsk Data, Oslo, Norway, pp. 1-12, Nov. 10, 1988
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ON	Boysel et al., "Four-Phase LSI Logic Offers New Approach to Computer Designer", Four-Phase Systems Inc. Cupertino, CA, Computer Design, April 1970, pp. 141-146,
ON	Boysel et al., "Random Access MOS Memory Packs More Bits To The Chip", Electronics, Feb. 16, 1970, pp. 109-146,

EXAMINER <i>Glenn Alne</i>	DATE CONSIDERED <i>5/16/2001</i>
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<i>GA</i>	5,034,964	Jul. 23, 1991	Khan et al. <i>DVR</i>	<i>—</i>	<i>—</i>	

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<i>GA</i>	Hansen et al., "A RISC MICROPROCESSOR WITH INTEGRAL MMU AND CACHE INTERFACE", MIPS Computer Systems, Sunnyvale, CA, IEEE 1986 pp 145-148
<i>GA</i>	Moussouris et al., "A CMOS PROCESSOR WITH INTEGRATED SYSTEMS FUNCTIONS", MIPS Computer Systems, Sunnyvale, CA, IEEE 1986 pp 126-130
<i>GA</i>	"LR2000 High Performance RISC Microprocessor Preliminary" LSI Logic Corp. 1988, pp. 1-15
<i>GA</i>	"LR2010 Floating Point Accelerator Preliminary" LSI Logic Corp. 1988, pp 1-20
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<i>GA</i>	Riordan T. "MIPS R2000 Processor Interface 78-00005(C)", MIPS Computer Systems, Sunnyvale, CA, June 30, 1987, pp 1-83
<i>GA</i>	Moussouris, J. "The Advanced Systems Outlook-Life Beyond RISC: The next 30 years in high-performance computing", Computer Letter, July 31, 1989 (an edited excerpt from an address at the fourth annual conference on the Advanced Systems Outlook, in San Francisco, CA (June 5))

EXAMINER <i>Glenn Auvre</i>	DATE CONSIDERED <i>5/16/2001</i>
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